CLAIMS

What is claimed is:

1. A sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

a material between the source and drain beneath the gate having a predetermined length; and

a detection device coupled to the drain by a signal path, wherein the material allows the detection device to be reset to a predetermined state.

2. The sensor of claim 1, further including an implant in the material that increases a surface threshold of the transistor.

3. The sensor of claim 2, wherein the surface threshold of the transistor is increased to at least 0.8 volts.

4. The sensor of claim 2, wherein the implant is in approximately a half of the length of the material.

5. The sensor of claim 3, wherein the half of the material is closest the detection device.

6. The sensor of claim 2, wherein the implant is boron.

7. The sensor of claim 2, wherein the predetermined length of the material is at least 20 percent greater than a process minimum.

8. The sensor of claim 2, wherein the drain is formed by a phosphorous implant level between $3e^{13}$ cm^{-3} and about $6e^{12}$ cm^{-3}.

9. The sensor of claim 2, wherein the gate has a gate length approximately two times a process minimum.

10. The sensor of claim 1, wherein the gate is divided into a p-type region and a n-type region.

11. The sensor of claim 10, wherein the predetermined length of the gate is approximately two times a process minimum.

12. The sensor of claim 10, wherein the material is a p-type material.

13. The sensor of claim 12, wherein the p-type substrate is in proximity to the p-type region of the gate.

14. The sensor of claim 10, wherein the drain is formed by a phosphorous implant level of approximately $2e^{12}$ cm^{-3}.

15. The sensor of claim 10, including an implant region located in the drain extending under the p-type region of the gate.

16. The sensor of claim 15, wherein the implant region is a surface boron implant region.

17. The sensor of claim 1, wherein the detection device is a photo-detector.

18. The sensor of claim 17, wherein the photo-detector is a photodiode.

19. A method for resetting a sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

increasing a potential that is required in order to deplete a channel associated with a material between the source and the drain under the gate;

depleting the channel between the source and drain in response to a tapered voltage applied to the gate overcoming the potential; and

draining a charge through the transistor from a detection device in response to the creation of the channel.

20. The method of claim 19, wherein increasing the potential further comprises implanting boron in the material between the source and the drain.

21. The method of claim 19, wherein increasing the potential further comprises increasing the surface threshold of the transistor by at least 0.8 volts.

22. The method of claim 19, wherein implanting boron further includes doping a half of the length of the material with boron.

23. The method of claim 22, wherein doping a half of the length of the material occurs in the material closest the detection device.

24. The method of claim 19, wherein creating a channel further includes forming a channel 20 percent greater than a process minimum.

25. The method of claim 19, wherein creating a channel further includes doping the drain with a phosphorus implant level between $3e^{13}$ cm^{-3} and about $6e^{12}$ cm^{-3}.

26. The method of claim 19, wherein increasing the surface threshold level of a material between the source and the drain under the gate further includes dividing the gate into a p-type region and a n-type region.

27. The method of claim 26, wherein the p-type region and the n-type region combined is approximately two time a process minimum in length.

28. The method of claim 26, wherein the p-type region and the n-type region combined in the gate has a gate length approximately two time a process minimum in length.

29. The method of claim 26, wherein increasing the potential further includes creating the drain with a phosphorous implant level of approximately $2e^{12}$ cm^{-3}.

30. The method of claim 26, wherein creating a channel further includes forming an implant region located in the drain extending under the p-type region of the gate.

31. The method of claim 30, wherein the implant region located in the drain contains Boron.

32. A sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

means for increasing a potential that is required in order to deplete a channel associated with a material between the source and the drain under the gate;

means for depleting the channel between the source and drain in response to a tapered voltage applied to the gate overcoming the potential; and

means for draining a charge through the transistor from a detection device in response to the creation of the channel.

33. The sensor of claim 32, wherein increasing means further comprises means for implanting a hole-increasing dopant in the material between the source and the drain.

34. The sensor of claim 33, wherein implanting means further includes a half of the length of the material being doped with the hole-increasing dopant.

35. The sensor of claim 34, wherein the half of the length of the material occurs in the material closest the detection device.

36. The sensor of claim 34, wherein the hole-increasing dopant is Boron.

37. The sensor of claim 32, wherein the increasing means increases the surface threshold of the transistor by at least 0.8 volts.

38. The sensor of claim 32, wherein the creating means further includes the channel having a channel length that is 20 percent greater than a process minimum.

39. The sensor of claim 32, wherein the creating means further includes means for doping the drain with an electron-increasing dopant implant level between $3e^{13}$ cm^{-3} and about $6e^{12}$ cm^{-3}.

40. The sensor of claim 39, wherein the electron-increasing dopant is Phosphorus.

41. The sensor of claim 32, wherein increasing means further includes means for dividing the gate into a p-type region and a n-type region.

42. The sensor of claim 41, wherein the p-type region and the n-type region combined is approximately two time a process minimum in length.

43. The sensor of claim 41, wherein the p-type region and the n-type region combined in the gate has a gate length approximately two time a process minimum in length.

44. The sensor of claim 41, wherein the increasing means further includes means for creating the drain with an phosphorous level of approximately $2e^{12}$ cm^{-3}.

45. The sensor of claim 41, wherein the creating means further includes means for forming an implant region located in the drain extending under the p-type region of the gate.

46. The sensor of claim 45, wherein the implant region located in the drain contains hole-increasing dopant.

47. The sensor of claim 46, wherein the hole-increasing dopant is boron.

48. The sensor of claim 32, wherein the detection device is a photo-detector.

49. The sensor of claim 48, wherein the photo-detector is a photodiode.